**Area Efficient ROM-Embedded SRAM Cache**

**Abstract**

There are many important applications, such as math function evaluation, digital signal processing, and builtin self-test, whose implementations can be faster and simpler if we can have large on-chip “tables” stored as read-only memories (ROMs). We show that conventional de facto standard 6T and 8T static random access memory (SRAM) bit cells can embed ROM  
data without area overhead or performance degradation on the bit cells. Just by adding an extra wordline (WL) and connecting the WL to selected access transistor of the bit cell (based on whether a 0 or 1 is to be stored as ROM data in that location), the bit cell can work both in the SRAM mode and in the ROM mode. In the proposed ROM-embedded SRAM, during SRAM  
operations, ROM data is not available. To retrieve the ROM data, special write steps associated with proper via connections load ROM data into the SRAM array. The ROM data is read by conventional load instruction with unique virtual address space assigned to the data. This allows the ROM-embedded cache (R-cache) to bypass tag arrays and translation look-aside buffers,  
leading to fast ROM operations. We show example applications to illustrate how the R-cache can lead to low-cost logic testing and faster evaluation of mathematical functions.

**Tools:**

* DSch
* Microwind

**Languages:** NA